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THEORY AND EXPERIMENTAL RESULTS OF FLYING-ADDER FREQUENCY SYNTHESIZER

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ABSTRACT

Flying-Adder frequency synthesis architecture is a comparatively new technique of generating fractional frequency derived from reference frequency. The first advantage is that system consists of pure digital circuits. The second advantage is fast response. On the other hand, this synthesizer generates a desired average frequency, which is not spectrally pure. Since its invention, it has been utilized in many commercial products. During the evolution of this architecture, the issues related to circuit and system level implementations have been studied in prior publications. In this paper, we attempt to present the signal characteristics in time and frequency domain based on another approach, which was not so far published. The theoretical results are confirmed by simulation and also supported by experimental results, gained through the construction of simple flying adder frequency synthesizer.

KEYWORDS: Direct Digital Synthesis, Fractional Synthesizer, Flying Adder, Frequency Synthesis, Phase Locked Loop, Sigma Delta, Time-Average-Frequency

INTRODUCTION

Flying-Adder architecture is a new concept time-average-frequency, to generate frequencies. The main advantage is that system consists of pure digital circuits and also fast response is important. Along the history of frequency synthesis development, Phase-Lock Loop (PLL) based synthesis method is the mostly used approach. Within this approach, there are several important points: Integer-N architecture, Fractional-N architecture and Sigma-Delta Fractional-N architecture. Integer-N PLL is commonly used in the cases where frequency requirement is straightforward. Fractional-N PLL is a technique which can generate output frequencies that are fractional multiples of the input reference frequency. This is important step forward from the Integer-N PLL. However, this advancement is accompanied with a serious drawback. It degrades the spectrum purity of the output frequency. To overcome this problem, Sigma-Delta Fractional PLL was developed [1-3]. For FAS some rigorous mathematical results, concerning this architecture has been published in [4-15]. FAS generate frequencies that are exact submultiplies of a fixed harmonic of the input reference frequency. And by using fractional techniques, it can generate average frequencies, with the jitter that accompanies these techniques, but it has no loop to reduce the jitter. Nevertheless, there are applications where the accurate average frequency of FAS is sufficient and where, therefore, the application can benefit from its pure digital nature.

The Flying-Adder architecture is interesting technique in the field of frequency synthesis. Unlike the conventional PLL, the FAS consists of digital circuitry such as multiplexers, adders, and flip-flops, thereby resulting in fast switching time and wide tuning range. The proof of FAS concept was constituted in 2000 [4]. It was built on the foundation of a new

concept: Time-Average-Frequency. The theoretical foundation was established in 2008 [5, 16-20]. The more in-depth study is delivered in [9, 10]. In this paper, the basic FAS is described and also, the FAS is used with conjunction of PLL. Compared to the pure structure FAS, the proposed approach can achieve the same frequency resolution with reduced fractional spurs.

The Flying-Adder Synthesizer Principle

The FAS [6, 7], which is also referred to as direct digital period synthesizer or digital-to-frequency converter, is an independent frequency synthesis. The FAS shares some functionality with circuits that involve phase-switching prescalers and digital phase accumulators [5]. Due to its wide tuning range and instant response time, the FAS frequency synthesizer is highly suitable for many System-on-Chip applications.

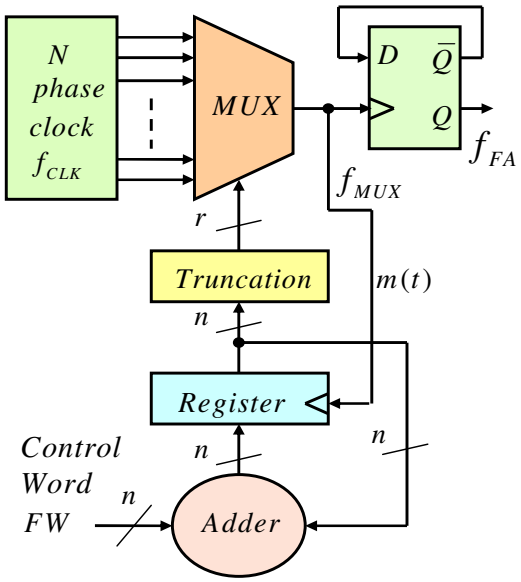

Figure 1: The Block Diagram of Fractional Flying Adder (FFA) Frequency Synthesizer Consist of: *N*-Phase Clock Generator (Frequency F_{clk}), Multiplexer MUX, D-Flip-Flop, Digital Adder with Control Frequency Word *FW*, Register and Truncation Which Convert *N*-Bit Word to *R*-Bit Word. Output Frequency of FFA Is F_{mux} OR $F_{fa} = F_{mux}$ /2

The block diagram of basic FAS is shown in Figure 1. All parts of this system is digital. The system is driven by the $N = 2^m$ clock phases with frequency f_{CLK}, 50 % duty-cycle square waves with phase shift $-2\pi/N$, one of which is selected by the *N*-to-1 multiplexer (*MUX*). The rising edges of *MUX*'s output (signal *m(t)*) is a trigger for the *n*-bit register changing its value from

$$x_{k+1} = (x_k + FW) mod 2^n \tag{1}$$

where *FW* is the *n*-bit long frequency control word and *k* is integer variable which presents counts of the rising edges of signal *m(t)*. The register value x_k, is then truncated by taking the first *r*, most significant bits to y_k according (2).

$$y_k = fix\left(\frac{x_k}{2^{n-m}}\right) \tag{2}$$

where function *fix(x.)* rounds the elements of *x* to the nearest integers towards zero. The y_k controls the *MUX* and

therefore chooses the input phase that passes through the *MUX*. The signals *m(t)* (with frequency f_{MUX}) which is a sequence of pulses, or spikes are fed to the D-Flip-Flop which acts as a frequency divider by-2 providing the output signal with frequency $f_{FA} = f_{MUX}/2$. FAS employ a multiphase generator to generate multiple clock signals evenly distributed in a full clock cycle. These same-frequency-but-different-phases clock signals are used to synthesize desired frequency. The synthesized signal is directly related to the phase difference e.g. $\Delta = \pi/4$ (for N=8) among the multiple outputs from the generator, see Figure 2. The 8 phase can be coded as hexadecimal numbers which can be stored in memory and periodically read. It is important to note that maximal value x_k, eq. (1) in *Register* is limited to 2^n-1 (function $mod 2^n$) and maximal value of y_k, eq. (2) is limited to 2^r-1. The average frequency f_{AV} is given by the following expression [17]:

$$\left.\begin{aligned} f_{AV} &= \frac{2^n}{2^n-(2^r-1)FW} f_{CLK} \\ for\ \ & 0 \le FW \le 2^{n-r} \\ f_{AV} &= \frac{2^n}{FW} f_{CLK} \\ for\ \ & 2^{n-r} \le FW < 2^n \end{aligned}\right\} \tag{3}$$

where N is the number of generator phases. According eq. (3) FAS architecture with an N-phase generator has a frequency range f_{AV} from f_{CLK} to $N \cdot f_{CLK}$ [17]. The average output frequency f_{AV} and average output period T_{AV} for N=8, n=5, f_{CLK}=1 and $FW \in \langle 0, 31 \rangle$ are shown in Figure 3. The average frequency is number of pulses within a given timeframe, e.g. one second. When FW is a fractional word (register value x_k, is truncated), the FAS modulate the output frequency. The frequency modulation results in spurious spikes in the frequency spectrum. It is important to note that for $0 \le FW < 2^{n-r}$ output signal *m(t)* with frequency f_{MUX} is strongly irregular with different length of pulses. Therefore usually the FW is used in range $2^{n-r} \le FW < 2^n$.

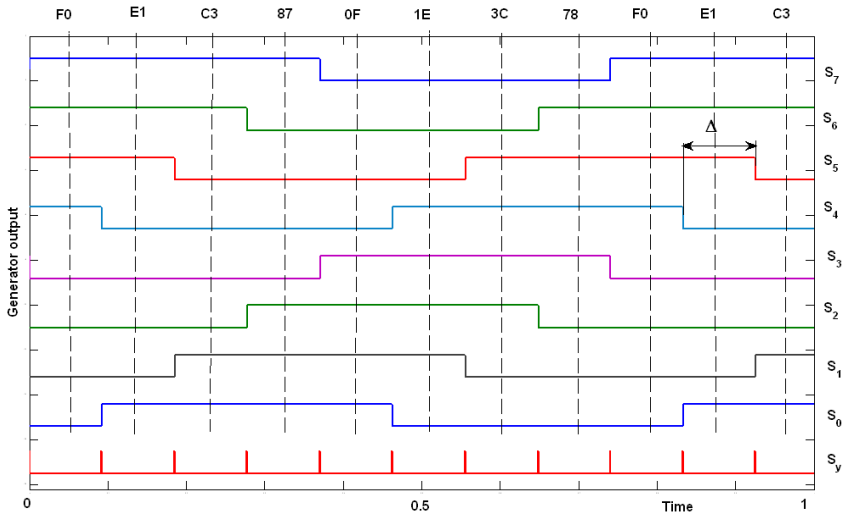

Figure 2: Example of Multiphase Generator (8 Phase Generator, N=8, S_1, S_2, S_3 … S_8 with Phase Difference Δ among the Multiple Outputs and Output Pulses S_o. the 8 Phase Can Be Coded as Hexadecimal Numbers (on the Top). the Output Pulses S_o Are Generated by Digital Edge Combiner Circuit on Rising Edges

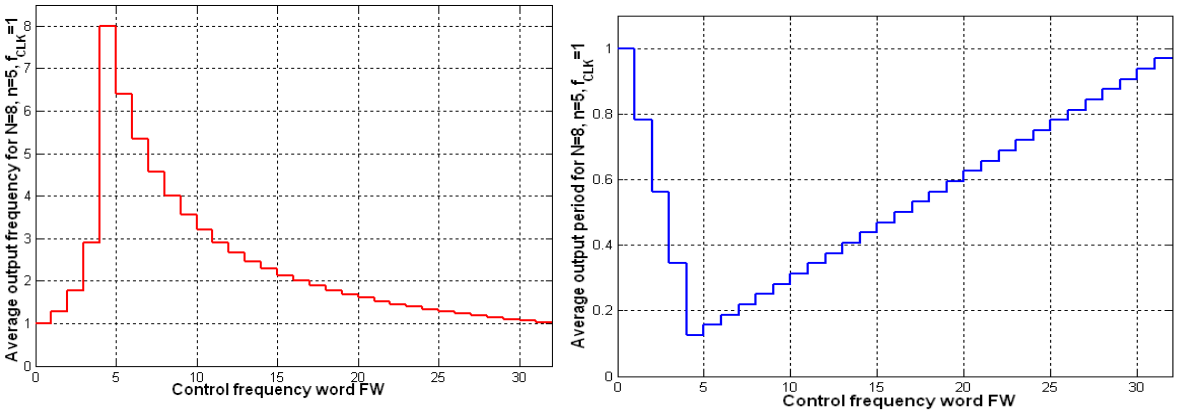

Figure 3: Average Frequency F_{av} (Left) and Average Period T_{AV} (Right) as Function of *FW*

The Flying-Adder Synthesizer Output Signal

In this part the detailed properties of output signal is derived, confirmed by simulation and by construction of simple FAS. For values: r=3, n=8 and f_{clk}=1/8 and $32 \le FW < 256$ ($2^{n-r} \le FW < 2^n$) average output frequency f_{AV} (according (3)) is

$$f_{AV} = \frac{2^n}{FW} f_{clk} = \frac{256}{FW}\frac{1}{8} = \frac{32}{FW}, \quad if \quad 32 \le FW < 256 \tag{4}$$

And average output period T_{AV}

$$T_{AV} = \frac{1}{f_{AV}} = \frac{FW}{32}, \quad if \quad 32 \le FW < 256 \tag{5}$$

For these conditions, the minimal T_{AV}=1. Output signal $m(t)$consists from set of pulse which has of different length T_1 and T_2 (for r=3, n=8 and f_{clk}=1/8) we have

$$T_2 = T_1 + \left(T_{AV}\right)_{\min} = T_1 + 1 \tag{6}$$

And T_1 is given by (7)

$$T_1 = fix\left(\frac{FW}{32}\right) \tag{7}$$

For given frequency word FW the Diophantine equations must be solved for computing numbers a and b (a>0, b>0) according eq. (8)

$$\begin{aligned} aT_1 + bT_2 &= aT_1 + b\left(T_1 + 1\right) = FW \\ a + b &= 2^{n-r} = 2^{8-3} = 32 \end{aligned} \tag{8}$$

After manipulations we receive

$$a = 32(T_1 + 1) - FW \quad \text{and} \quad b = 32 - a \tag{9}$$

And final numbers a_1 and b_1 are given by

$$a_1 = \frac{a}{\gcd(a,b)}, \qquad b_1 = \frac{b}{\gcd(a,b)} \tag{10}$$

where function *gcd(x,y)* is the greatest common divisor of corresponding elements of x and y. Output signal consist of a_1 pulses of period T_1 and b_1 pulses of period T_2, therefore repeated period (pattern which repeats indefinitely) is

$$T_r = a_1 + b_1 \tag{11}$$

But output signal is divided in several combination pattern of T_1 and T_2 (pulses) depending on a_1, b_1 according (12)

$$\begin{aligned} &if\ b_1 = 0 \ \Rightarrow\ g_1 = 1 \\ &if\ a_1 = 1\ or\ b_1 = 1 \ \Rightarrow\ g_1 = \frac{\max(a_1,b_1)}{\min(a_1,b_1)} = \max(a_1,b_1) \\ &if\ a_1 \neq 1\ and\ b_1 \neq 1 \ \Rightarrow\ g_1 = fix\left(\frac{\max(a_1,b_1)}{\min(a_1,b_1)}\right), \quad g_2 = g_1 + 1 \end{aligned} \tag{12}$$

where g_1 and g_2 are length of pattern of repeated pulses.

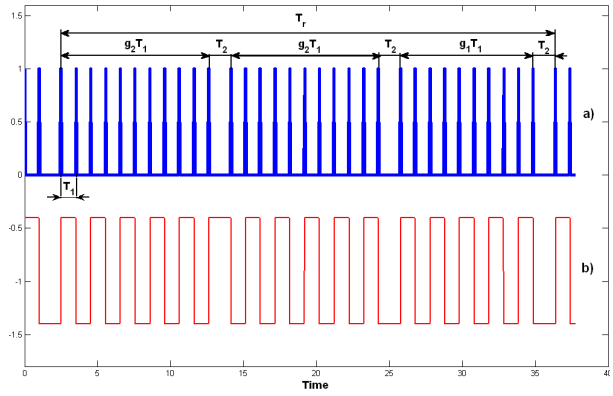

Figure 4: Signals for *FW*=35, *R*=3, *N*=8 and F_{clk}=1/8: A) MUX Output and Signal *M* (*T*) Divided by 2 B) Output of D-Flip-Flop. Repeated Period T_r Consists of Following Pulses (G_1=9; G_2=10) $T_r = 10T_1+T_2+10T_1+T_2+9T_1+T_2$ where $T_2=T_1+1=10T_1+T_2+10T_1+T_2+9T_1+T_2$ where $T_2=T_1+1$

Example 1. Output signal *m(t)* calculation for *FW*=35 (*r*=3, *n*=8 and f_{clk}=1/8)

T_1=*fix*(35/32)=1; $T_2=T_1+1$; a=32(1+1)-35=29; b=32-29=3; *gcd*(29,3)=1; a_1=29; b_1=3. Therefore output signal repeated period T_r=32 consists of 29 pulses of T_1 and 3 pulses of T_2. From eq. (12) we calculate g_1=9 and g_2=10 and because total number of pulses T_1 is 29, we must solve Diophantine equation

$$xg_1 + yg_2 = 9x + 10y = 29, \qquad x, y > 0 \tag{13}$$

After solving eq. (13) we receive x=1, y=2. Output pulses distribution is shown in Figure 4. The repeated period T_r consists of following combination pattern of T_1 and T_2:

$T_r = 10T_1+T_2+10T_1+T_2+9T_1+T_2$

The simulation from Figure 4 was confirmed by measuring on constructed of FAS (FAS was constructed by

means of microcontroller, n=8, N=8, f_{CLK}=1kHz), see scope of output signals, Figure 5. The numerical results for other FW are shown in Tab. 1(on the end of paper). From Tab. 1 can be seen that e.g. for FW=32 output pulse is only T_1=1 (a=32, b=0), therefore ideal 50 % duty-cycle square wave without period jitter. The same is for FW=0, 64, 96, 128, 160, … (FW=32*n, where n=0, 1, 2…7) but T_1 is increasing. The similar (the same pulse pattern) is for other values of FW, e.g. distribution of output pulses are the same for $FW \in$ [35; 67; 99; 131…], but with increasing lengths of T_1 and T_2. Output signals and spectrum for FW=35, r=3, n=8 and f_{clk}=1 kHz for constructed FAS is shown in Figure 6 and for FW=32 in Figure 7.

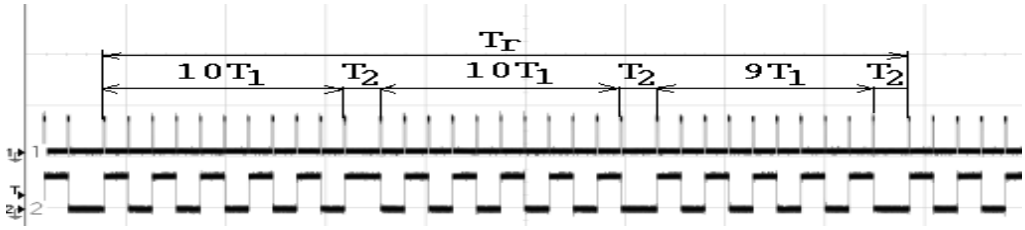

Figure 5: Scope of Measuring on Constructed FAS for: FW=35, R=3, N=8 and F_{clk}=1 Khz. Signal $M(T)$ on MUX Output (Channel 1) and Signal $M(T)$ Divided By 2 (Channel 2). Repeated Period T_r Consists of Following Pulses: T_r =10T_1+T_2+10T_1+T_2+9T_1+T_2 Where T_2=T_1+1

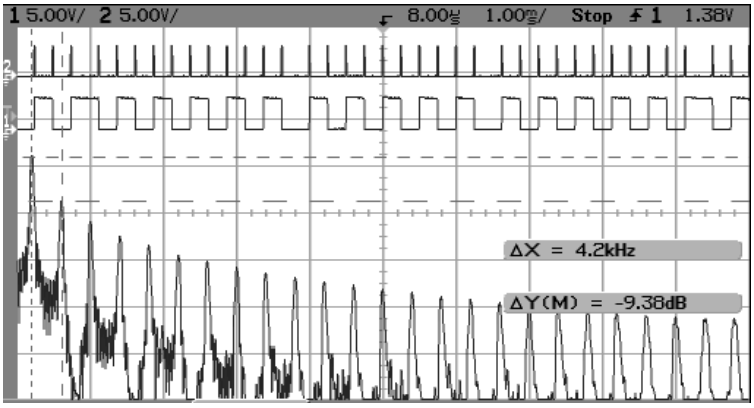

Figure 6: Output Signals (Channel 2-Top Signal at MUX Output,Channel 1 – D Flip-Flop Output) And Frequency Spectrum of Channel 1 for FW=35, R=3, N=8 and F_{clk}=1 Khz

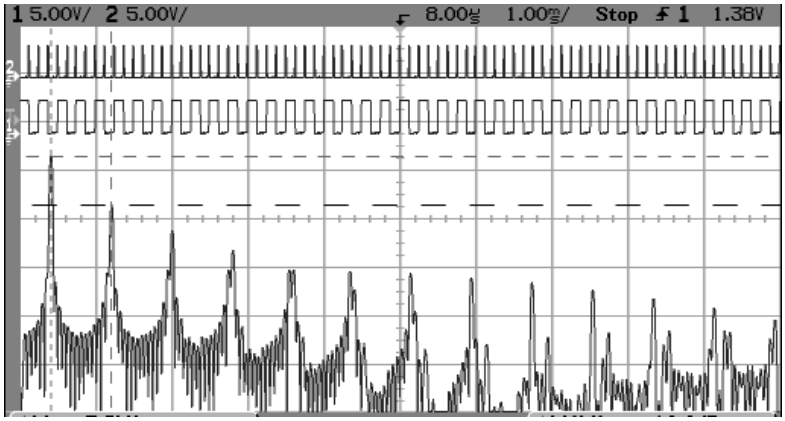

Figure 7: Output Signals (Channel 2-Top Signal at MUX Output, Channel 1 – D Flip-Flop Output) and Frequency Spectrum of Channel 1 for FW=32, R=3, N=8 and F_{clk}=1 Khz

Table 1: FAS Results for Different *FW* Column of "Output Pulses" Mean: [$9T_1$; T_2;$10T_1$;T_2;$10T_1$;T_2]= $9T_1+1T_2+10T_1+1T_2+10T_1+1T_2$

Fw	T_1	T_2	*A*	*B*	A_1	B_1	F_{av}	Repeated Period T_r	Output Pulses Distribution
32	1	2	32	0	32	0	32/32	T_1	[T_1]
33	1	2	31	1	31	1	32/33	$31*T_1+1*T_2$	[$31T_1$; T_2]
34	1	2	30	2	15	1	32/34	$15*T_1+1*T_2$	[$15T_1$; T_2]
35	1	2	29	3	29	3	32/35	$29*T_1+3*T_2$	[$9T_1$;T_2;$10T_1$;T_2;$10T_1$;T_2]
36	1	2	28	4	7	1	32/36	$7*T_1+1*T_2$	[$7T_1$; T_2]
...	...	...	...	...	...	...	...	...	...
63	1	2	1	31	1	31	32/63	$1*T_1+31*T_2$	[T_1; $31T_2$]
64	2	3	32	0	32	0	32/64	T_1	[T_1]
65	2	3	31	1	31	1	32/65	$31*T_1+1*T_2$	[$31T_1$; T_2]
66	2	3	30	2	15	1	32/66	$15*T_1+1*T_2$	[$15T_1$; T_2]
67	2	3	29	3	29	3	32/67	$29*T_1+3*T_2$	[$9T_1$;T_2;$10T_1$;T_2;$10T_1$;T_2]
...	...	...	...	...	...	...	...	...	...
127	3	4	1	31	1	31	32/127	$1*T_1+31*T_2$	[T_1; $31T_2$]
128	4	5	32	0	32	0	32/128	T_1	[T_1]
129	4	5	31	1	31	1	32/129	$31*T_1+1*T_2$	[$31T_1$; T_2]
...	...	...	...	...	...	...	...	...	...
253	7	8	3	29	3	29	32/253	$3*T_1+29*T_2$	[T_1;$9T_2$;T_1;$10T_2$;T_1;$10T_2$]
254	7	8	2	30	1	15	32/254	$1*T_1+15*T_2$	[T_1; $15T_2$]
255	7	8	1	31	1	31	32/255	$1*T_1+31*T_2$	[T_1; $31T_2$]

The Dithering Effect in Flying-Adder Synthesizer

One of the crucial parameters associated with the quality of a clock signal is the jitter. Jitter is generally defined as the timing uncertainty of the clock signal's rising or falling edge. It is a variable which is usually cannot be precisely predicated in real application environment. In real application environment, jitter is caused by uncontrollable or unforeseeable factors. On the other hand, by definition, all the edges of time-average-frequency clock signal are deterministic therefore they must be controllable in generation and predictable in utilization. In the case of FAS, there are only two types of cycles: type-T_1 and type-T_2. Type-T_2 is one Δ longer than type-T_1. Unlike jitter, this determinist can be taken into account beforehand when this type of clock signal is used to drive electronic systems but in some applications periodic generation of T_1 and T_2 can product the spurious signals which should be suppressed. The one simple method is converting the spurs line to noise by dithering (add the special modulation signal to *FW*) [20-25]. This scheme is depicted in Figure 8. The dithering signal d_S is added to *FW*. The best of all is use random number, but sawtooth or triangular signal can be also used. In all types of modulation, the DC component is zero. The simulation results for FAS *FW*=19, *r*=3, *n*=5 and f_{clk}=0.5 and spectrum of D-flip-flop output are shown in Figure 9, 10 and 11. In Figure 9, the spectrum of system without dithering is shown. In Figure 10, the spectrum of system with random number used for dithering (with variance =0.1). The random numbers are rounded to numbers -1,0,+1 and added to *FW*. In Figure 11 the sawtooth signal is used for spread spectrum generation.

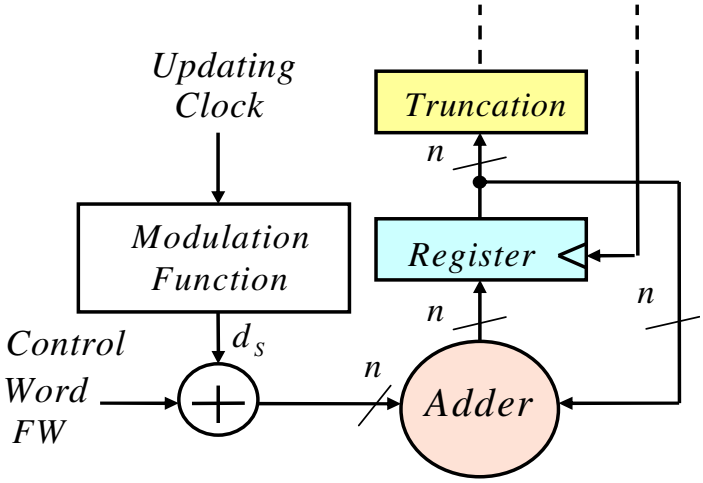

Figure 8: The Block Diagram of Dithering (Added in FAS). Output Signal of Modulation Function Block d_S is Add to *FW*

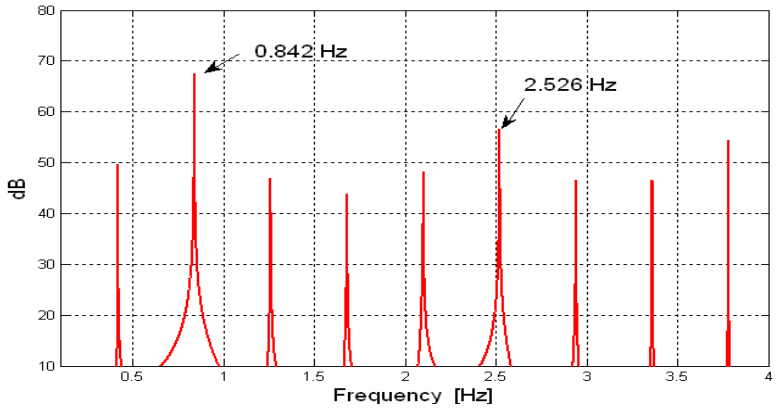

Figure 9: The Spectrum of FAS without Dithering

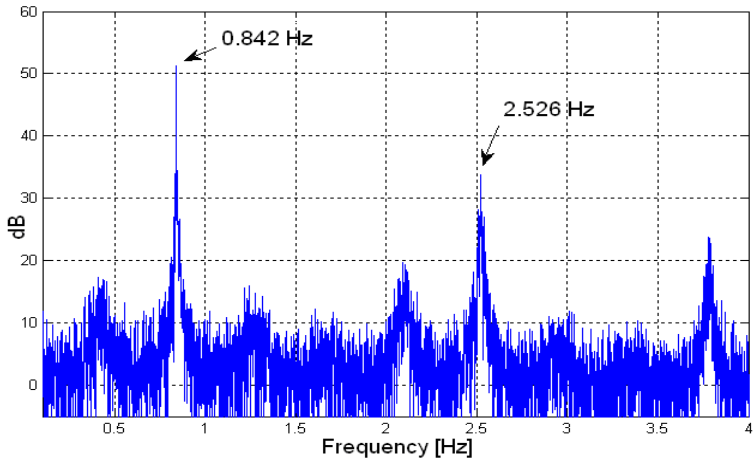

Figure 10: The Spectrum of FAS with Random Number Dithering (Mean=0, Variance =0.1)

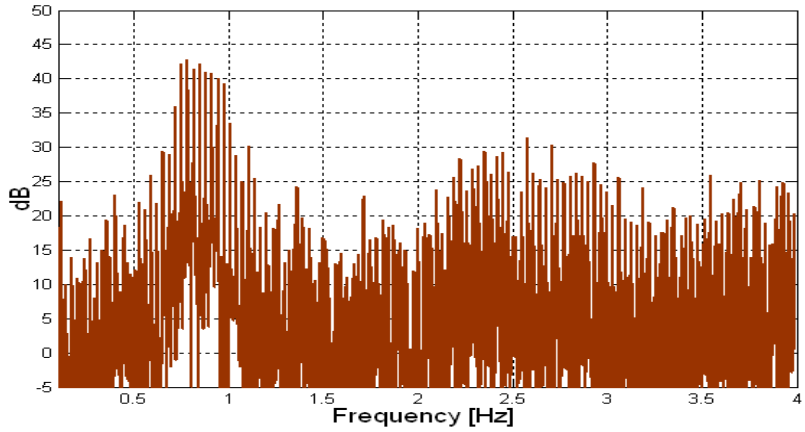

Figure 11: The Spectrum of FAS with Sawtooth Dithering

The Flying-Adder Synthesizer with Pll

In this part the FAS and PLL are used for spurious spectral line suppression [7, 15, 21]. The block diagram of the proposed fractional frequency synthesizer based on flying adder principle and PLL is shown in Figure 12.

The synthesizer consists of: Reference clock (with frequency f_R), charge-pump phase detector, *N*-phase voltage controlled oscillator with frequency f_{VCO} (controlled by voltage V_{VCO}), multiplexer *MUX*, frequency divider (divide input frequency f_{FA} by number *D*), digital adder with control frequency word *FW*, register and truncation which convert *n*-bit word to *r*-bit word. Output frequency of FAS is f_{FA}. The synthesizer output frequency (generated by edge combiner) is f_{OUT}. Suppose, that all system is in lock state, therefore reference frequency f_R and frequency on the output of frequency divider f_{FA}/D are the same

$$f_R = \frac{f_{FA}}{D} \tag{14}$$

Frequency f_{FA} for $0 \le FW \le 2^{n-r}$ is given

$$f_{FA} = \frac{2^n}{2^n - (2^r - 1)FW} f_{VCO} \tag{15}$$

And for $2^{n-r} \le FW < 2^n$

$$f_{FA} = \frac{2^n}{FW} f_{VCO} \tag{16}$$

After manipulation, using eq. (14) $\Rightarrow f_{FA}=D \cdot f_R$) for $0 \le FW \le 2^{n-r}$ f_{VCO} is

$$f_{VCO} = \frac{2^n - (2^r - 1)FW}{2^n} Df_R \tag{17}$$

and for $2^{n-r} \le FW < 2^n$

$$f_{VCO} = \frac{FW}{2^n} Df_R \tag{18}$$

On the end, output frequency f_{OUT} generated by edge combiner from N-phase VCO signal is $f_{OUT}=N.f_{VCO}$ and therefore for $0 \leq FW \leq 2^{n-r}$

$$f_{OUT} = \frac{2^n - (2^r - 1)FW}{2^n} NDf_R \tag{19}$$

and for $2^{n-r} \leq FW < 2^n$

$$f_{OUT} = \frac{FW}{2^n} NDf_R \tag{20}$$

where f_R is frequency of reference oscillator, D is divider number, N-number of phases of voltage controlled oscillator, n is number of register bits and FW is control word.

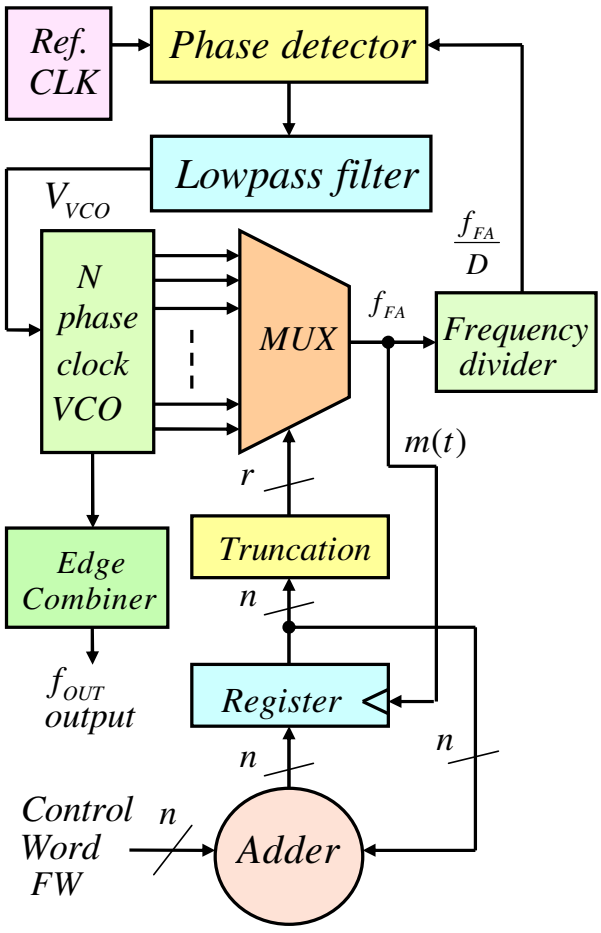

Figure 12: The Block Diagram of Second Type Fractional Frequency Synthesizer Based on PLL and FAS Principles. The Synthesizer Consists of: Reference Clock, *N*-Phase Voltage Controlled Oscillator (Controlled By V_{VCO}), Multiplexer MUX, Frequency Divider (Divide by Number D), Digital Adder with Control Frequency Word *FW*, Register and Truncation Which Convert N-Bit Word to *R*-Bit Word. Output Frequency of FAS Is F_{fa}. the Synthesizer Output Frequency Is F_{out}

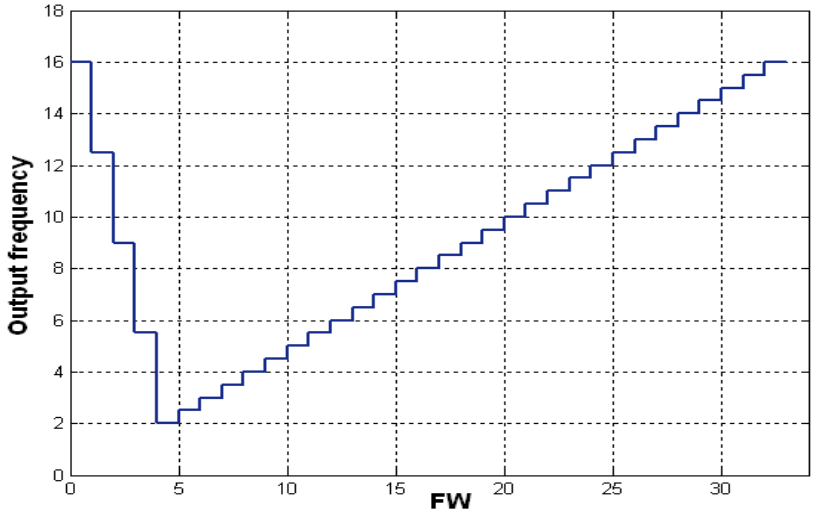

Figure 13: The Frequency on the Output of Edge Combiner for D=4, N=8, N=5, F_r=0.5 versus FW

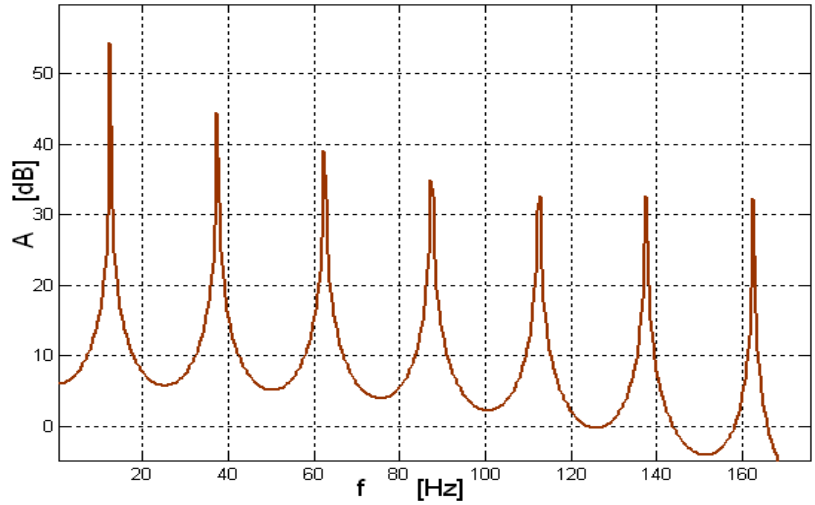

Figure 14: The Spectrum on the Output of Edge Combiner for FW=25 and F_r=0.5, D=4, N=8 And N=5

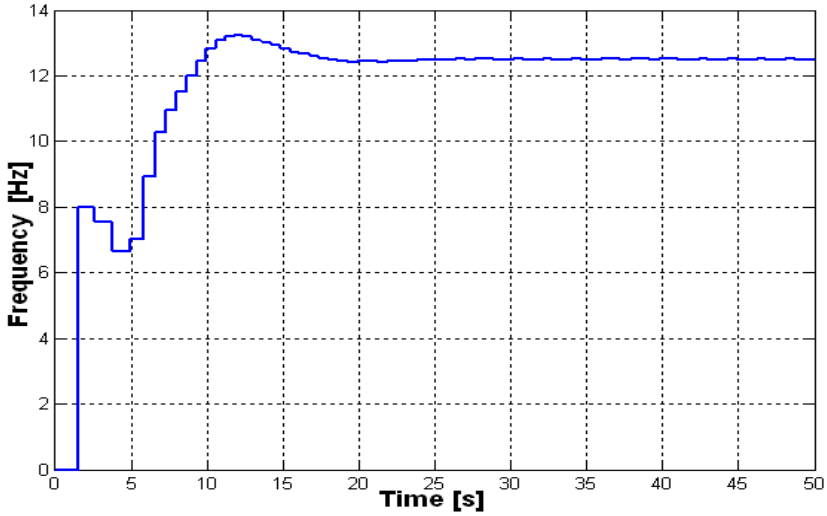

Figure 15: The Time Response of the Frequency Synthesizer for FW=25 And F_r=0.5, D=4, N=8, N=5 and 4-Th Order Low-Pass Filter

The output frequency as function of FW for f_R=0.5, D=4, N=8 and n=5 is shown in Figure 13. The example of frequency spectrum for FW=25 and f_R=0.5, D=4, N=8 and n=5 is shown in Figure 14 (for $f_{OUT}=(FW/2^n)NDf_R=(25/32)*8*4*0.5=12.5$ [Hz], square wave). The time response of the frequency synthesizer for FW changed to 25 and f_R=0.5, D=4, N=8, n=5 and 4-th order low-pass filter is shown in Figure 15. The time response of the PLL (voltage output of 4-th order low-pass filter), is displayed in Figure16.

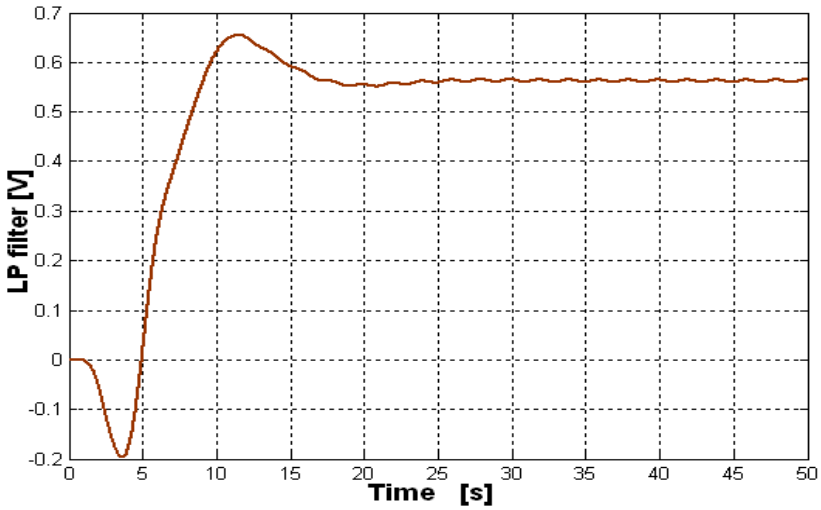

Figure 16: The Low-Pass Filter Time Response of the Frequency Synthesizer for FW=25 and F_r=0.5, D=4, N=8, N=5 and 4-Th Order Low-Pass Filter

CONCLUSIONS

Flying-Adder architecture is an innovative method for frequency synthesis. The effeteness of this technique has been proven by many commercial products in the past few years. The great advantage is that Flying-Adder architecture consists of pure digital circuitry such as multiplexers, adders, and flip-flops, thereby resulting in fast switching time, wide tuning range and therefore enables simple programmable logic construction. In this paper in the first part, a simple Flying-Adder frequency synthesizer has been presented, simulated, constructed and measured. The new approach for output signal pattern was derived and main properties of this synthesizer were described. In the second part, the new Flying-Adder technique in cooperation with Phase Locked Loop was derived and simulated. The trade-off of this approach is that Flying-Adder loses its "instant response" advantage, because the low-pass filter is included in system. In future, all-digital frequency synthesizer consists of Flying-Adder and PLL can be developed.

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